

Silicon N-Channel Planar Power MOSFET

Description

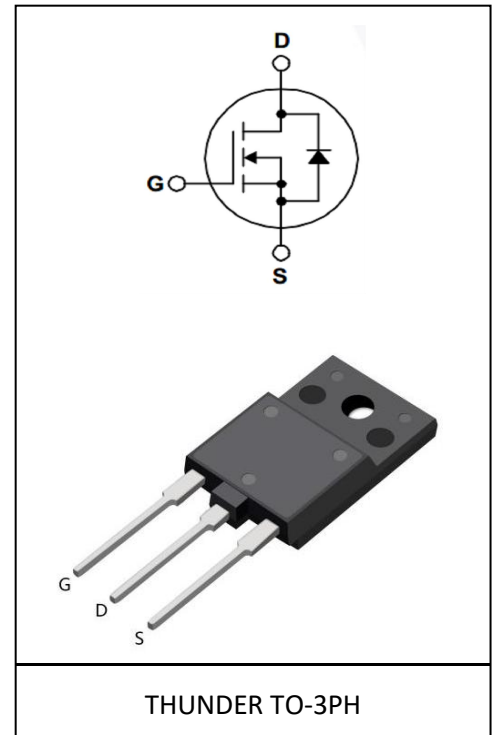
The TH4N120PH utilizes the latest processing techniques to achieve low on-resistance per silicon area. Additional features of this MOSFET are 150°C operating junction temperature and high repetitive peak current capability. These features combine to make this MOSFET a highly efficient, robust and reliable device for PDP driving applications. It can be used in a wide variety of applications.

General Features

- $V_{DS}=1200V, I_D=4A$
- Low ON Resistance, $R_{DS(on), typ.}=3.2\Omega @ V_{GS}=10V, I_D=2A$
- Low reverse transfer capacitance
- Low Qg for fast response
- Short fall & rise times for fast switching
- 100% single pulse avalanche energy Test

Application

- Adaptor
- Charger
- SMPS Standby Power



Product Summary

V_{DS}	1200V
$R_{DS(on), typ.}$	3.2Ω
I_D	4A

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain-source voltage	V_{DS}	1200	V
Continuous drain current $T_C = 25^\circ C$ (Silicon limit)	I_D	4	A
Pulsed drain current ($T_C = 25^\circ C$, t_p limited by T_{jmax})	I_{DM}	16	A
Avalanche energy, single pulse ($L=10mH$, $R_g=25\Omega$)	E_{AS}	308	mJ
Gate-Source voltage	V_{GS}	±30	V
Power dissipation ($T_C = 25^\circ C$)	P_D	187	W
Operating junction and storage temperature	T_j, T_{stg}	-55...+150	°C

Thermal Resistance

Parameter	Symbol	Max	Unit
Thermal resistance, junction – case.	R_{thJC}	0.67	°C/W
Thermal resistance, junction – ambient(min. footprint)	R_{thJA}	62	

Electrical Characteristic (at $T_j = 25\text{ }^{\circ}\text{C}$, unless otherwise specified)

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		

Static Characteristic

Drain-source breakdown voltage	BV_{DSS}	1200	-	-	V	$V_{GS}=0V, I_D=250\mu A$
Gate threshold voltage	$V_{GS(th)}$	2.5	-	4.5	V	$V_{DS}=V_{GS}, I_D=250\mu A$
Zero gate voltage drain current	I_{DSS}	-	-	1	μA	$V_{DS}=1200V, V_{GS}=0V$ $T_j=25^{\circ}\text{C}$
		-	-	10	μA	$V_{DS}=960V, V_{GS}=0V$ $T_j=125^{\circ}\text{C}$
Gate-source leakage current	I_{GSS}	-	-	± 100	nA	$V_{GS}=\pm 30V, V_{DS}=0V$
Drain-source on-state resistance	$R_{DS(on)}$	-	3.2	3.8	Ω	$V_{GS}=10V, I_D=2A$
Transconductance	g_{fs}	-	4.0	-	S	$V_{DS}=40V, I_D=2A$

Dynamic Characteristic

Input Capacitance	C_{iss}	-	1272	-	pF	$V_{GS}=0V, V_{DS}=25V,$ $f=1\text{MHz}$
Output Capacitance	C_{oss}	-	105	-		
Reverse Transfer Capacitance	C_{rss}	-	13	-		
Gate Total Charge	Q_g	-	21	-	nC	$V_{GS}=10V, V_{DS}=960V,$ $I_D=4A$
Gate-Source charge	Q_{gs}	-	4.3	-		
Gate-Drain charge	Q_{gd}	-	10	-		
Turn-on delay time	$t_{d(on)}$	-	16	-	ns	$V_{DD}=600V, I_D=4A,$ $R_G=25\Omega$
Rise time	t_r	-	5	-		
Turn-off delay time	$t_{d(off)}$	-	25	-		
Fall time	t_f	-	13	-		
Gate resistance	R_G	-	1.525	-	Ω	$V_{GS}=0V, V_{DS}=0V,$ $f=1\text{MHz}$

Body Diode Characteristic

Parameter	Symbol	Value			Unit	Test Condition
		min.	typ.	max.		
Body Diode Forward Voltage	V_{SD}	-	-	1.5	V	$V_{GS}=0V, I_{DS}=4A$
Body Diode Continuous Forward Current	I_S	-	-	4	A	$T_C=25^{\circ}C$
Body Diode Reverse Recovery Time	t_{rr}	-	210	-	ns	$T_C=25^{\circ}C, I_S=4A,$ $di/dt=100A/us$
Body Diode Reverse Recovery Charge	Q_{rr}	-	765	-	nC	

Typical Performance Characteristics

Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

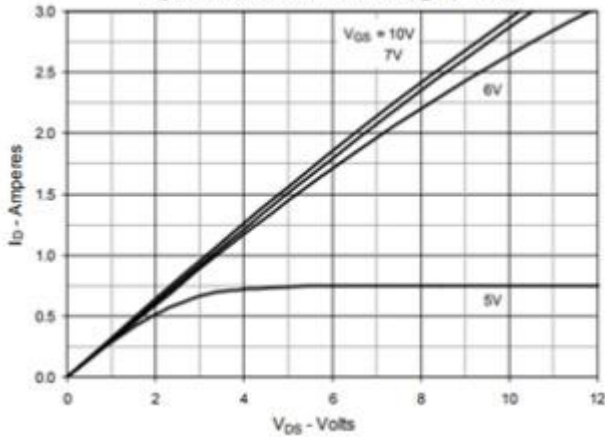


Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

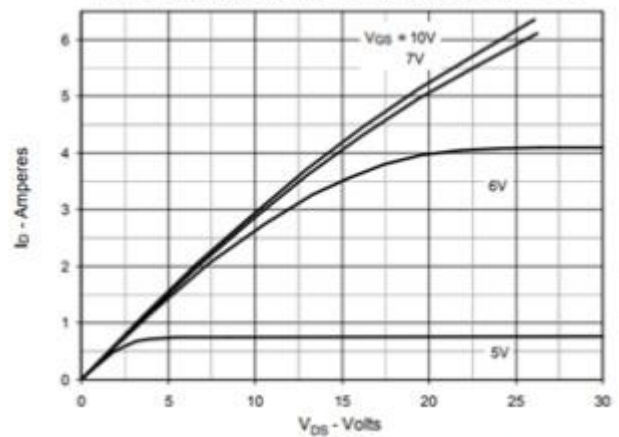


Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

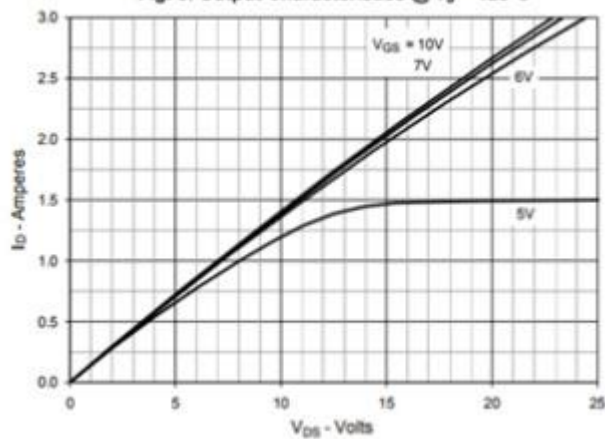


Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 2\text{ A}$ Value vs. Junction Temperature

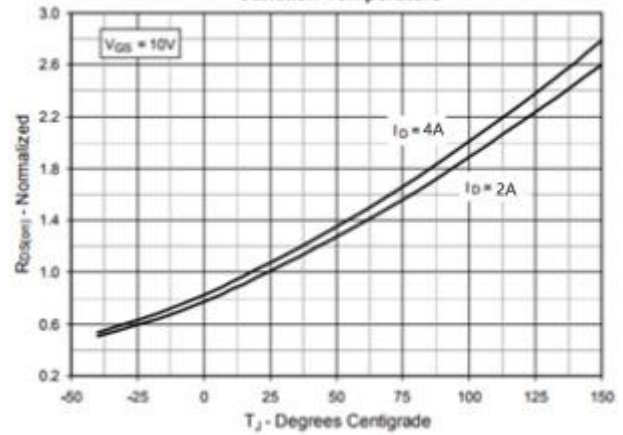


Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 2\text{ A}$ Value vs. Drain Current

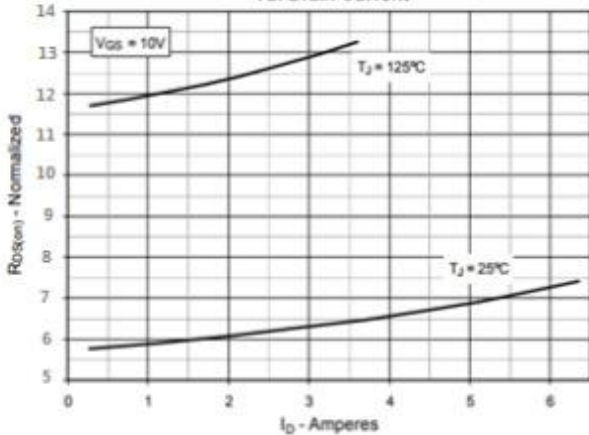


Fig. 6. Maximum Drain Current vs. Case Temperature

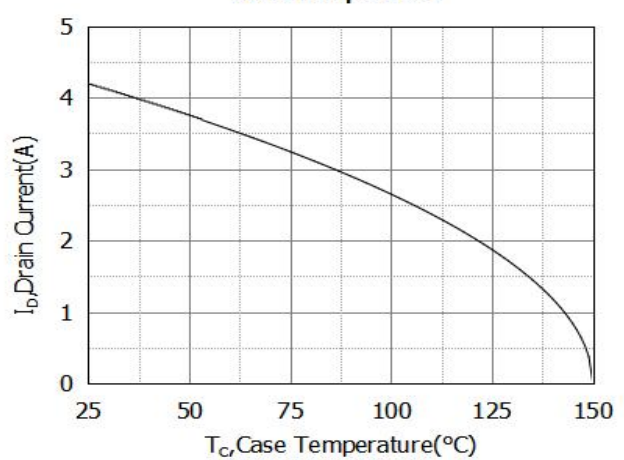


Fig. 7. Input Admittance

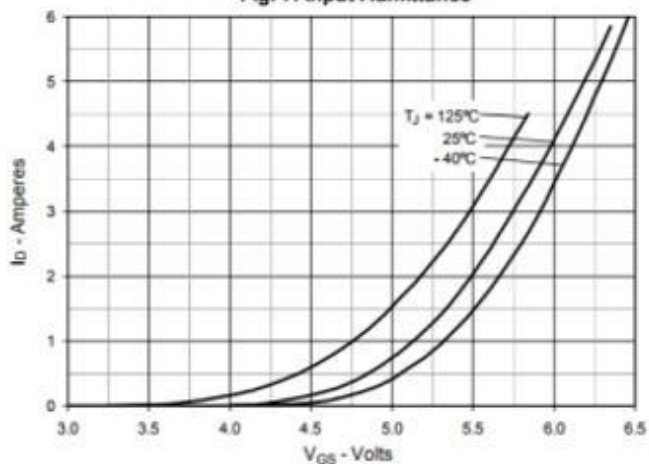


Fig. 8. Transconductance

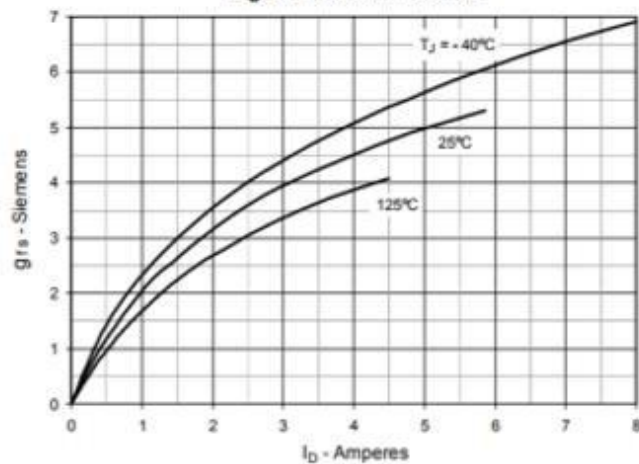


Fig. 9. Forward Voltage Drop of Intrinsic Diode

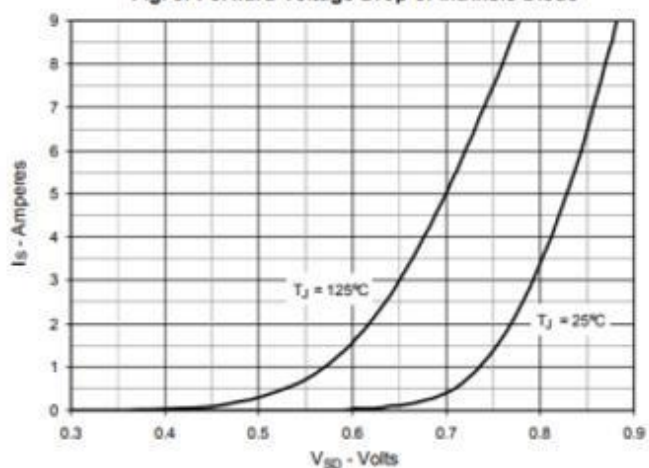


Fig. 10. Gate Charge

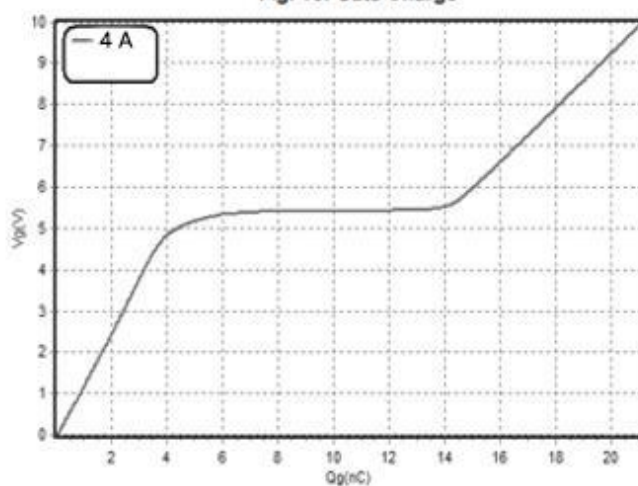


Fig. 11. Capacitance

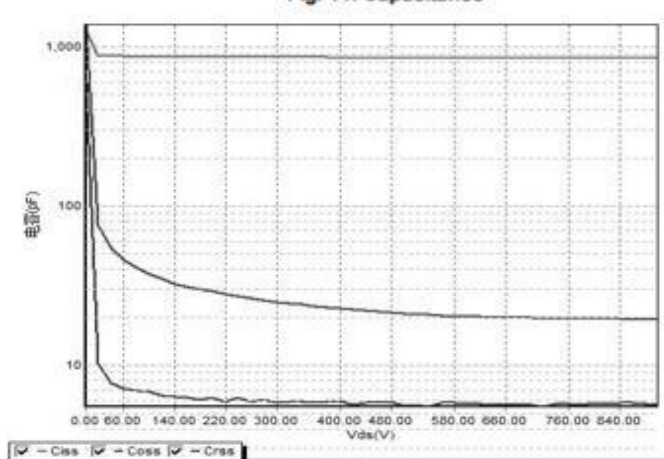


Fig. 12. Forward-Bias Safe Operating Area

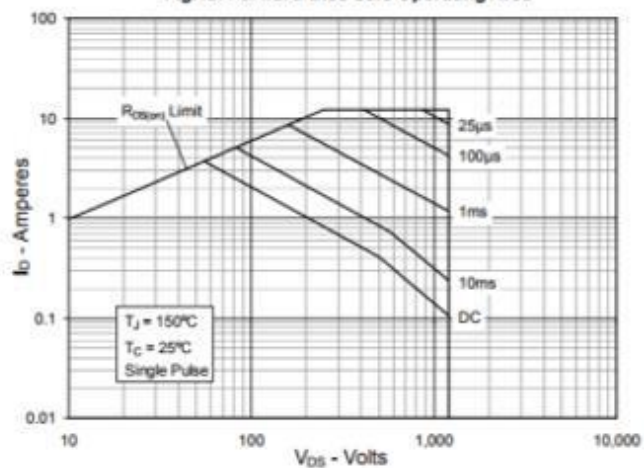
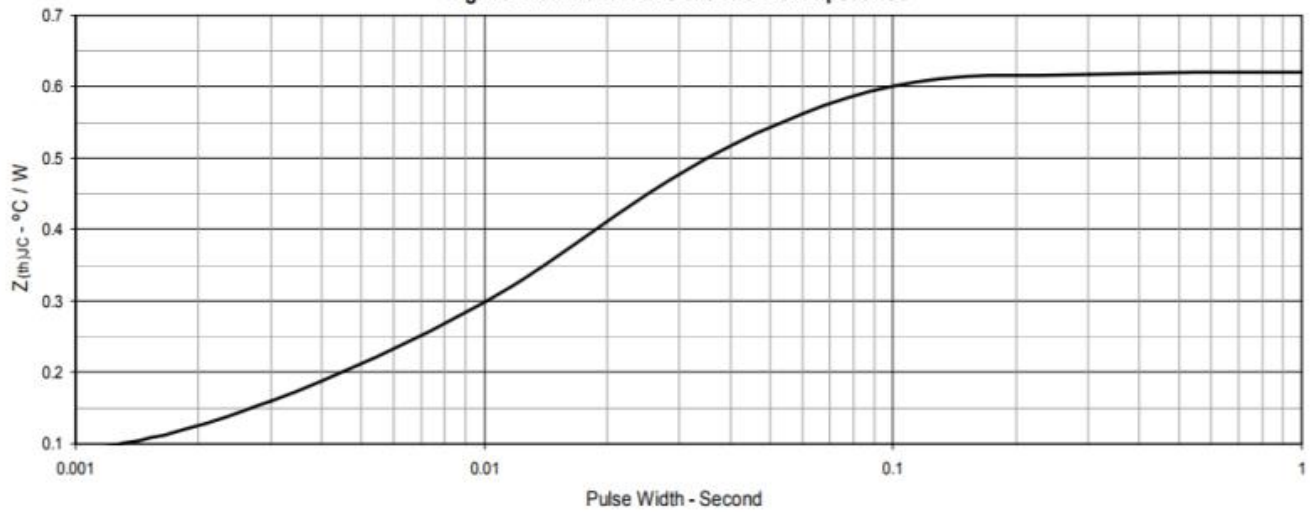


Fig. 13. Maximum Transient Thermal Impedance



Test Circuits and Waveforms

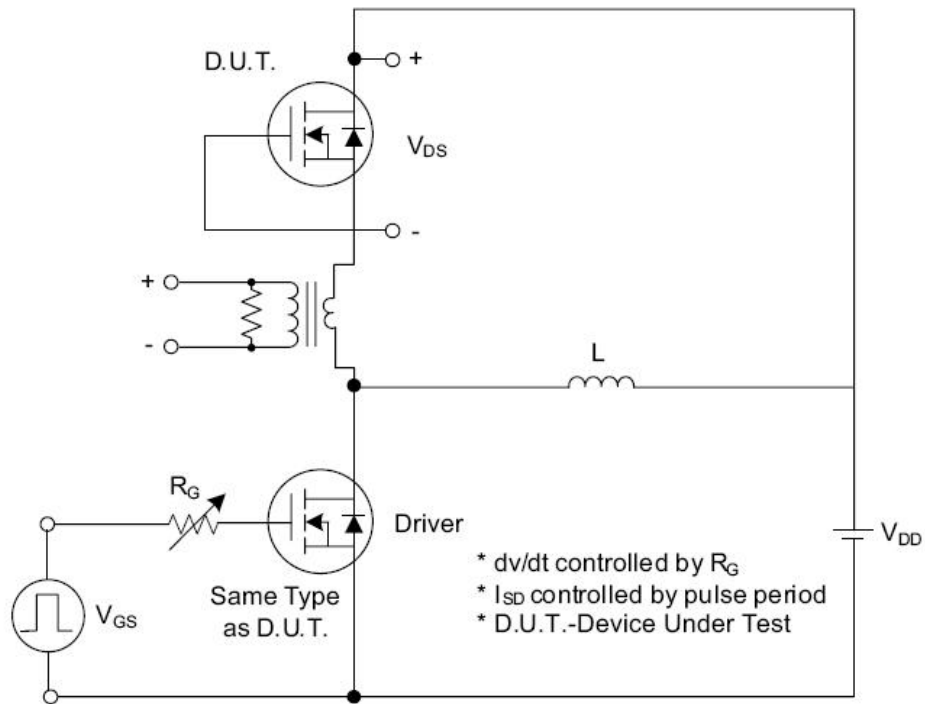


Fig. 1.1 Peak Diode Recovery dv/dt Test Circuit

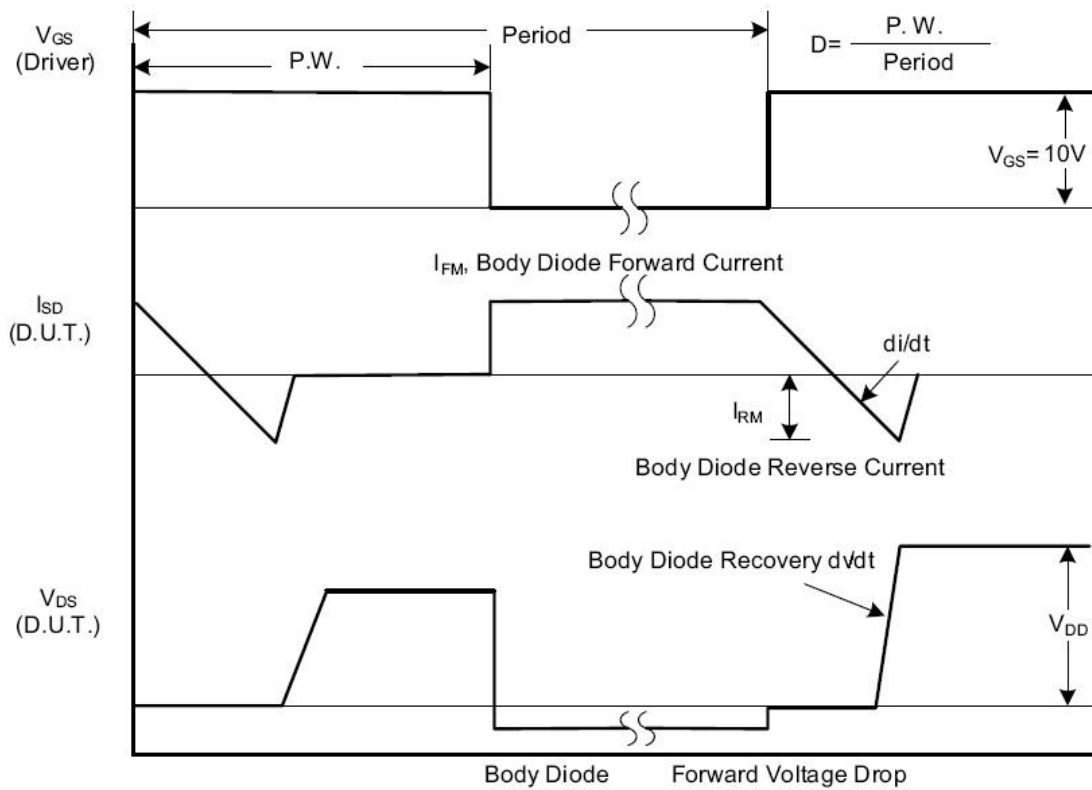


Fig. 1.2 Peak Diode Recovery dv/dt Waveforms

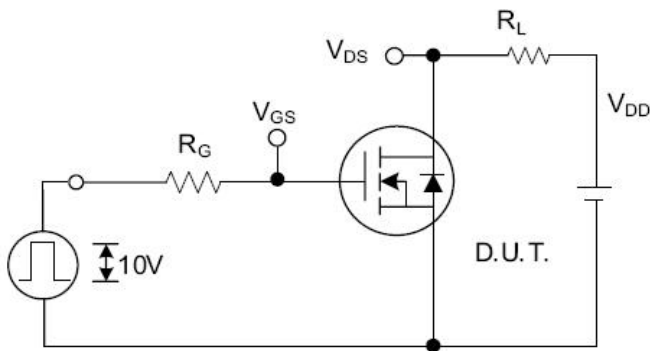


Fig. 2.1 Switching Test Circuit

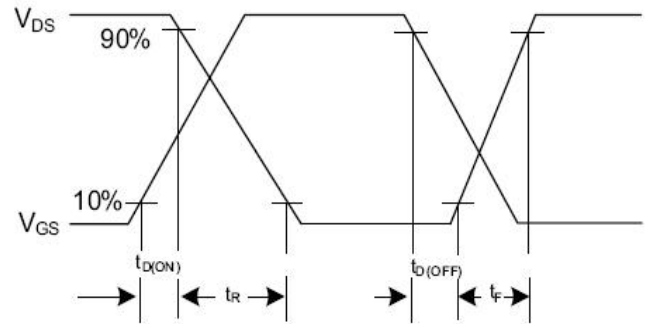


Fig. 2.2 Switching Waveforms

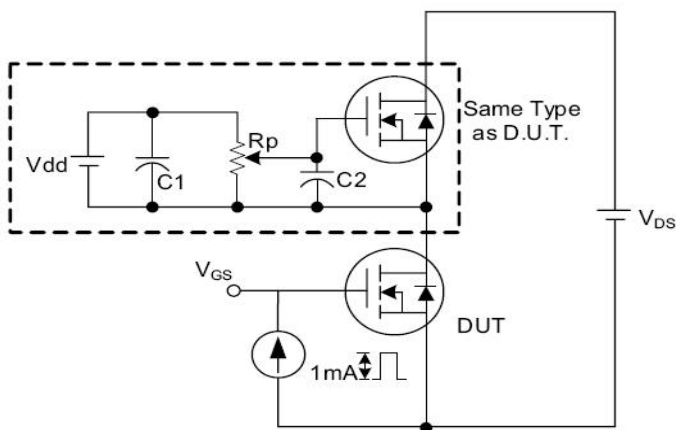


Fig. 3.1 Gate Charge Test Circuit

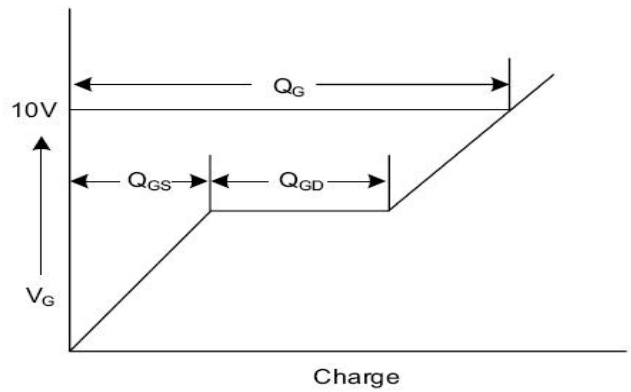


Fig. 3.2 Gate Charge Waveform

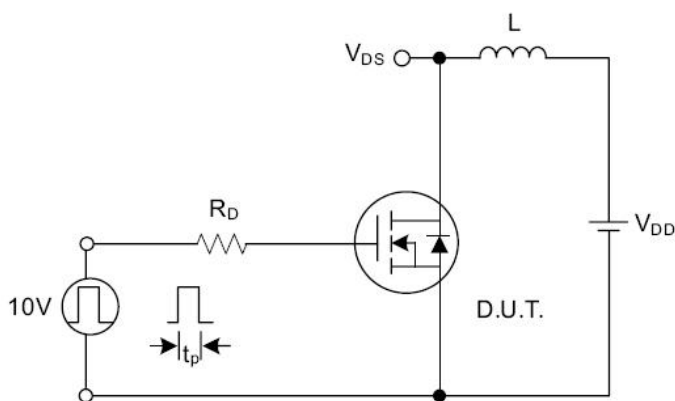


Fig. 4.1 Unclamped Inductive Switching Test Circuit

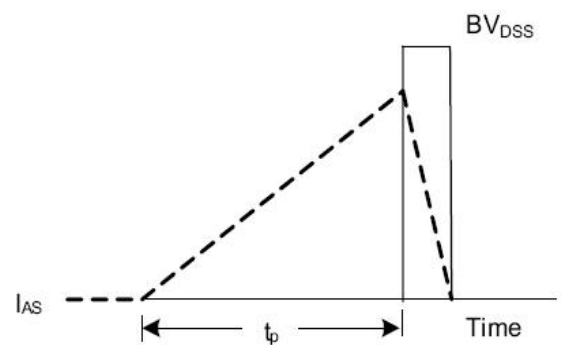
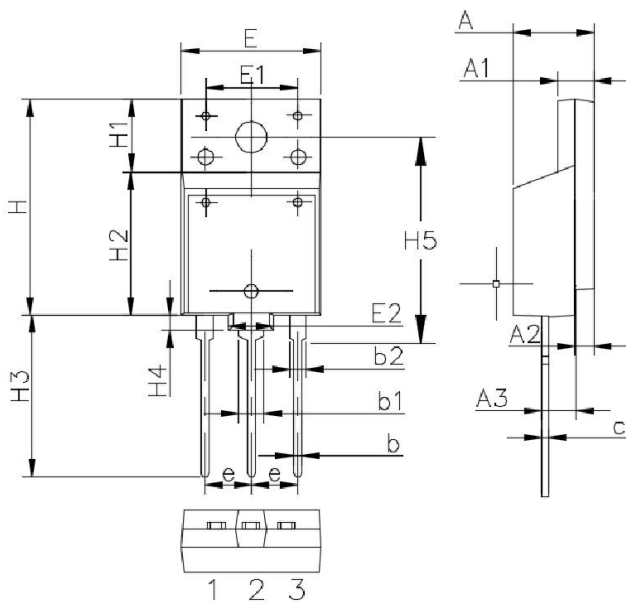


Fig. 4.2 Unclamped Inductive Switching Waveforms

Package Information

TO-3PH PACKAGE

基本尺寸



Symbol	单位 mm		
	Min	Nom	Max
A	5.35	5.55	5.75
A1	2.80	3.00	3.20
A2	1.90	2.10	2.30
A3	1.00	1.20	1.40
b	0.80	0.90	1.00
b1	1.80	2.00	2.20
b2	1.80	2.00	2.20
c	0.70	0.90	1.10
e	5.25	5.45	5.65
E	15.2	15.4	15.6
E1	9.80	10.0	10.2
E2	3.80	4.00	4.20
H	24.3	24.5	24.7
H1	9.80	10.0	10.2
H2	14.3	14.5	14.7
H3	18.5	19.0	19.5
H4	2.00	2.20	2.40
H5	24.0	24.5	25.0
G	4.3	4.5	4.7
ΦP	3.30	3.50	3.70

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